IN THE CLAIMS:

Please **cancel claims 1-7 and 9** without prejudice or disclaimer, **amend claim 8** as indicated below, and **add claims 10-15** as follows:

1-7. (*Cancelled*)

8. (*Currently amended*) A method of interfacing a data storage device comprising an array of a plurality of memory elements, with a logical address bus on which a plurality of logical address data is carried for identifying data stored in said memory device, said method comprising the steps of:

storing a data translation table comprising a plurality of data entries, each said data entry comprising a look up logical address value being a logical address stored in said data translation table and a look up physical address value, said look up physical address value corresponding to a physical location of one or more said memory elements;

upon receipt of a requested logical address, parsing said data entries in said data table, to read a look up logical address of each of a plurality of said data entries;

comparing said look up logical address with said requested logical address;

if a said look up logical address is less than said requested logical address, continuing to parse said data translation table; and

if a said look up logical address is ~~greater~~ less than ~~or equal to~~ said requested logical address, determining a corresponding respective physical address to said requested logical address as being said requested logical address, minus a look up logical address of a preceding data entry in said data translation table, plus a look up physical address corresponding to said preceding data entry in said data translation table.

9. (*Cancelled*)

10. (*New*) Apparatus for converting between a logical address of a data storage device, and a physical address corresponding to individual memory elements within said data storage device, said apparatus comprising:

a store for storing address data describing a plurality of logical addresses and a plurality of physical addresses, wherein each of said logical addresses corresponds to a respective physical address and is assigned an index value; and

a processor for:

(a) reading logical address request data describing a logical address of data to be retrieved;

(b) reading said stored address data and comparing said read logical address with a said stored logical address data at a first said index value;

(c) incrementing said index value if said logical address of said data to be retrieved is greater than or equal to a look up logical address corresponding to said index of said data entry;

(d) repeating steps (a), (b) and (c); and

(e) determining a physical address corresponding to said logical address to be retrieved as the sum of the physical address of the previous data entry and the difference between the logical address to be retrieved and the logical address of the previous data entry.

11. (*New*) Apparatus for interfacing a data storage device including an array of a plurality of memory elements, with a logical address bus for carrying a plurality of logical address data for identifying data stored in said memory device, said apparatus comprising:

a store for storing a plurality of data entries, each of said data entries comprising a look up logical address value that is a logical address stored in said store and a look up physical address

value, said look up physical address value corresponding to a physical location of one or more said memory elements; and

a processor for:

(a) parsing said data entries in said data table, to read a look up logical address of each of a plurality of said data entries in response to receipt of a requested logical address;

(b) comparing said look up logical address with said requested logical address;

(c) continuing to parse said data translation table if said look up logical address is less than said requested logical address; and

(d) if said look up logical address is less than said requested logical address, determining a corresponding respective physical address to said requested logical address as being said requested logical address, minus a look up logical address of a preceding data entry in said data translation table, plus a look up physical address corresponding to said preceding data entry in said data translation table.

12. (*New*) Apparatus for interfacing a data storage device including an array of a plurality of memory elements, with a logical address bus for carrying a plurality of logical address

data for identifying data stored in said memory device, said apparatus comprising:

a store for storing a plurality of data entries, each of said data entries having an index number, a logical address value and a physical address value, said physical address value corresponding to a physical location of one or more of said memory elements; and

a processor for:

(a) detecting at least one defective memory element;

(b) locating, in said store, a pair of entries, that define a range of physical address encompassing the address of the defective memory element;

(c) inserting two additional entries in said store between said pair of entries;

(d) creating a first additional data entry in said store, said first additional data entry comprising a logical address which corresponds to the first defective element of the group of defective elements and a physical address being that of a group of previously unused (spare) storage elements; and

(e) creating a second additional data entry in said store, said second data entry comprising the logical address corresponding to the physical address subsequent to the highest addressed element

of the group of defective elements and that same physical address as the physical address.

13. (*New*) A memory storing a program for enabling a processor to convert between a logical address of a data storage device, and a physical address corresponding to individual memory elements in said data storage device, the computer being arranged to be used with a store for storing address data describing a plurality of logical addresses and a plurality of said physical addresses, wherein each said logical address corresponds to a respective physical address and is assigned an index value, the program being in the memory causing the computer to:

(a) read logical address request data describing a logical address of data to be retrieved;

(b) read said stored address data and compare said read logical address with a said stored logical address data at a first said index value;

(c) increment said index value if said logical address of said data to be retrieved is greater than or equal to a look up logical address corresponding to said index of said data entry;

(d) repeat steps (a), (b) and (c); and

(e) determine a physical address corresponding to said logical address to be retrieved as being the sum of the physical address of

the previous data entry and the difference between the logical address to be retrieved and the logical address of the previous data entry.

14. (*New*) A memory storing a program for enabling a processor to interface a data storage device having an array of a plurality of memory elements, with a logical address bus for carrying a plurality of logical address data for identifying data stored in said memory device, the computer being arranged to be used with a store for storing a plurality of data entries, each of said data entries comprising a look up logical address value that is a logical address stored in said store and a look up physical address value, said look up physical address value corresponding to a physical location of one or more said memory elements, the program stored in the memory causing the computer to:

(a) parse said data entries in said data table to read a look up logical address of each of a plurality of said data entries upon receipt of a requested logical address;

(b) compare said look up logical address with said requested logical address;

(c) continue to parse said data translation table if said look up logical address is less than said requested logical address; and

(d) if said look up logical address is less than said requested logical address, determining a corresponding respective physical address to said requested logical address as being said requested logical address, minus a look up logical address of a preceding data entry in said data translation table, plus a look up physical address corresponding to said preceding data entry in said data translation table.

15. (*New*) A memory storing a program for enabling a processor to interface a data storage device having an array of a plurality of memory elements, with a logical address bus for carrying a plurality of logical address data for identifying data stored in said memory device, the computer being arranged to be used with a store for storing a plurality of data entries, each of said data entries comprising an index number, a logical address value and a physical address value, said physical address value corresponding to a physical location of one or more said memory elements, the program stored in the memory causing the computer to:

(a) detect at least one defective memory element;

(b) locate, within said store, a pair of entries which define a range of physical addresses encompassing the address of the defective memory element;

(c) insert two additional entries in said store between said pair of entries;

(d) create a first additional data entry in said store, said first additional data entry having a logical address which corresponds to the first defective element of the group of defective elements and a physical address being that of a group of previously unused or spare storage elements; and

(e) create a second additional data entry in said store, said second data entry having the logical address corresponding to the physical address subsequent to the highest addressed element of the group of defective elements and that same physical address as the physical address.